Circuit Analysis Homework 4

Professor: Brian Frost

Fall 2019

1. Consider the source-free RL circuit in Figure 1. Assume an initial current I_0 at time $t = 0$. For positive time, find the current through this circuit.

2. Classify the response derived above as one of natural, forced, or a mixture of the two. No explanation needed.

3. How much energy is stored in the inductor at $t = 0$?

4. Find a formula for power absorbed by the resistor for time $t > 0$, and then find the total energy absorbed by the resistor in all positive time.

5. Consider the simple step response circuit in Figure 2. Assume that the capacitor is initially charged to some voltage V_0. Solve for the voltage across the capacitor as a function of time, and isolate the natural and forced responses of the circuit.

6. There are three possible cases in the above problem – V_0 can be less than, equal to or greater than V. Roughly sketch the capacitor voltages in these three cases in time.

7. Consider the more complex first order circuit in Figure 3 – solve for the capacitor voltage as a function of time assuming its voltage is 0 at time $t = 0$. Sketch this voltage, and sketch the current source's current in time.

8. Consider the series RLC circuit in Figure 4. With initial current I_0 and initial capacitor voltage V_0, find the conditions for the circuit to be critically damped, overdamped and underdamped. Show work, don't just spit out results we derived in class! Draw the current in time for each of these responses roughly.

9. Suppose the initial capacitor voltage in Figure 5 is V_0. Find the conditions under which this circuit's response is critically damped, underdamped and overdamped where the output is considered to be the capacitor voltage. What is the steady state capacitor voltage for positive time?

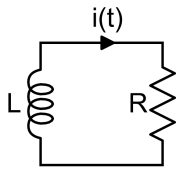

Figure 1: A source-free RL circuit

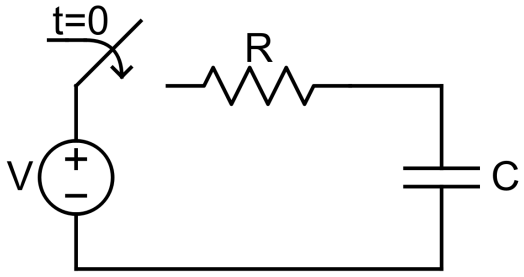

Figure 2: A simple step response circuit

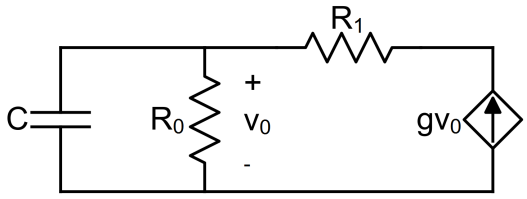

Figure 3: A first order circuit

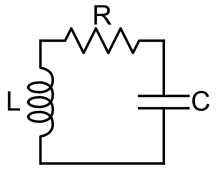

Figure 4: A source-free series RLC circuit

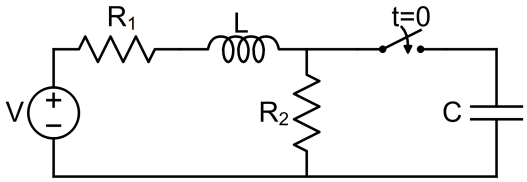

Figure 5: A second order circuit